SECTION 4
THEORY OF OPERATION

4.1 GENERAL

This section provides a detailed description of the functions and Theory of Operation of the 6900K series TWTAs. Detailed schematic diagrams for each of the major subassemblies defined in this section are included in Section 6 of this manual and should be used for reference in the following text descriptions.

NOTE

The reference designations used in the discussions in this section are the same as those on the applicable schematic. The reader should be aware of the fact that the complete reference designation usually requires a prefix to fully identify each component. For example, the full reference designation of chassis mounted capacitor C1 would be UD1C1 which is usually written as 1C1. Similarly, capacitor C1 on the Power Processor Assembly (A2) is fully identified as 1A2C1. Within the text for a particular assembly, the simplified reference (e.g. C1) is used for components included in that assembly and the full reference designation is used for components external to the assembly being discussed.

Understanding the Theory of Operation of the TWT Amplifier is a necessity for the technician who will maintain the equipment and an asset for the operator. A thorough understanding of the Theory of Operation of the equipment provides more efficient operation and quicker and more effective repairs, if problems should develop. This section (as well as the guidelines on high voltage and microwave radiation that are contained in the Supplementary Data Section) should be completely understood before the performance of any maintenance activity on the system.

All the available standard options are covered in the discussion of the Theory of Operation of the TWTA even if such options are not included in your specific TWTA (See Section 1.0). Special features (nonstandard options) are discussed separately in the Special Features Section of the manual.

4.2 FUNCTIONAL DESCRIPTION

A simplified block diagram of the Power Amplifier (PA) is shown in Figure 4-1. While all of the TWTA components are mounted in a single drawer assembly, it is convenient to discuss the unit in terms of the Power Supply Section, GPIB Interface Section, and the RF Section. Section 4.2 briefly discusses the functions of the Power Supply and RF sections. Detailed discussions are presented in Section 4.3.

4.2.1 Power Supply Functions

The Power Supply section is designed to accommodate a family of Varian Associates Traveling Wave Tubes (TWTs) with CW RF output power levels ranging from 1 to 20 Watts. The major functions of the Power Supply Section are:

A. Prime Power Interface Circuits: These circuits provide the interface between the prime power source and the Power Processor PCB Assembly. 115 VAC, 60 Hz is standard with an option for 230 VAC operation available. The prime power interface circuits include input fusing and RFI filtering required to couple the prime power source (115 VAC or optional 230 VAC) to the Power Supply circuits.

B. High Voltage and Bias Power Supplies: These functions are implemented with two major assemblies, the Power Processor PCB Assembly and the High Voltage Assembly.

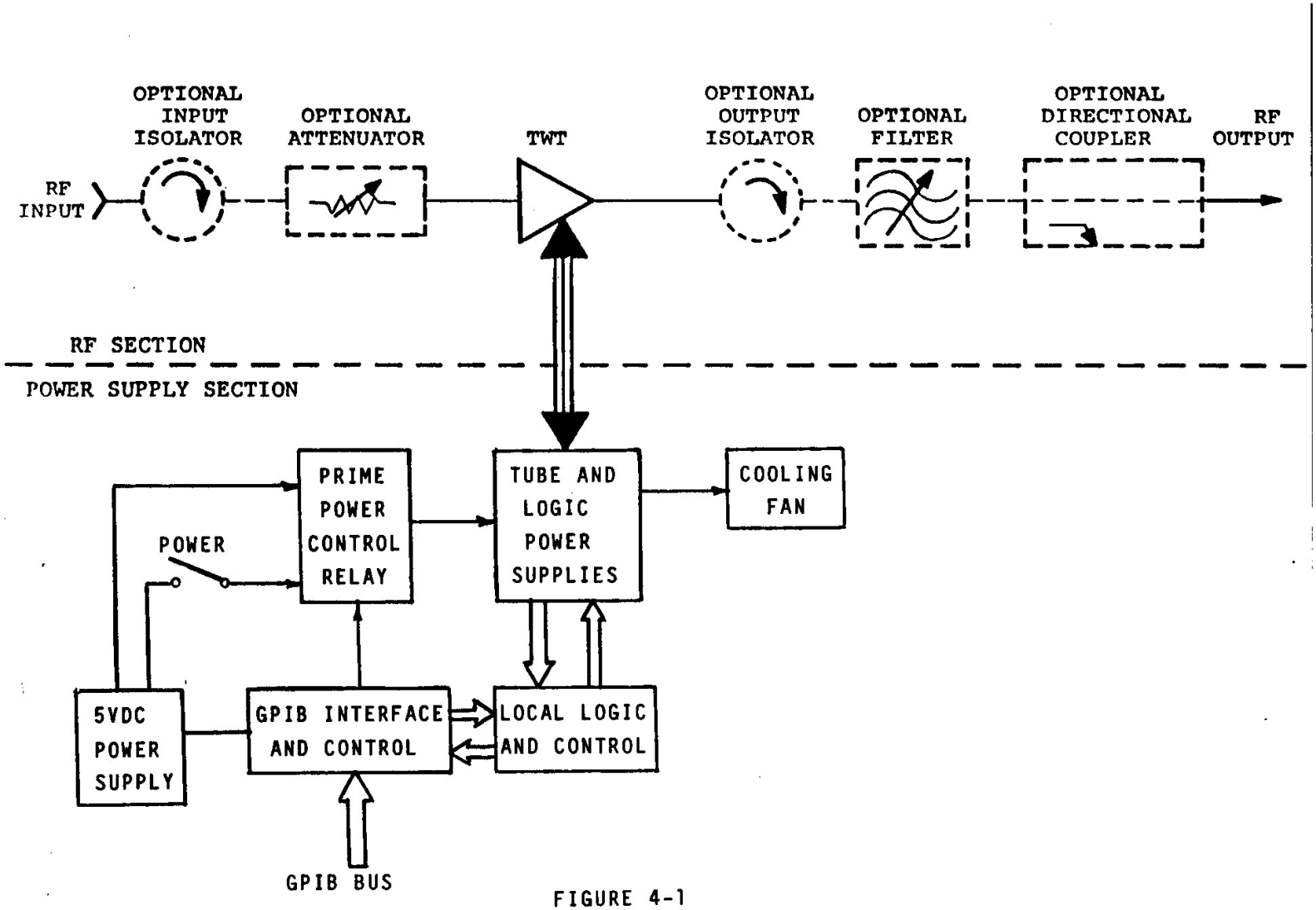


FIGURE 4-1

FUNCTIONAL BLOCK DIAGRAM - POWER AMPLIFIER

1031-1/85

This portion of the Power Supply circuitry accepts the outputs of the Prime Power Interface circuits and converts prime power into:

1. The regulated low voltage supplies needed by the protection, control, and indication circuitry.

2. The high voltage well-regulated supplies required for the TWT.

3. The low voltage supply needed for the cooling fan.

4. The low voltage supply needed for power conversion for the high voltage supply.

5. Grid or anode voltages when required for some of the tube options.

C. Control and Indicator Functions: This portion of the Power Supply provides the circuitry and switches required for control of prime power, TWT high voltage and the optional Local/Remote interface. Status indications are provided that show the operating state of the TWTA and when certain faults occur. A metering function that displays helix current is also provided. An Optional Elapsed Time Meter is available.

D. Cooling: Cooling air is provided by a small fan mounted on the rear of the TWTA. The dominant source of heat within the TWTA is the TWT which is cooled through a heat exchanger by the air flow from the cooling fan. Before entering the heat exchanger duct, most of the air passes across the power supply circuitry to provide cooling.

4.2.2 GPIB Remote Interface Function

This function is accomplished through the GPIB assembly and a front panel GPIB Control Assembly. The interface allows control and monitoring of the primary TWTA functions via a GPIB and a remote terminal. Refer to Section 3.3 for detailed operation and implementation data for the GPIB control.

4.2.3 RF Section Function

The function of the RF Section is to amplify RF signals in the frequency range of interest, consistent with the specifications for the model purchased. The TWT is the active element and exhibits nominal gains of 30 to 54 dB over a relatively wide frequency spectrum. The user has a number of RF options available. The RF Section is designed to accommodate all of these RF options. The available options allow input and/or output isolation, manual control of TWTA RF gain, output filtering and output/reflected power sampling.

4.3 DETAILED DISCUSSION OF POWER SUPPLY SECTION

Figure 4-2 is a block diagram of the Power Supply Section. The Power Supply Section consists of the Prime Power Interface Circuits; the Power Processor PCB Assembly; the cooling fan; the High Voltage Assembly; an optional Grid Supply PCB Assembly; an optional Anode Supply PCB Assembly; (the grid and anode supplies are only installed with certain tube options); the control, fault detection and indicator logic; and the Remote Control Interface.

4.3.1 Prime Power Interface

The function of the Prime Power Interface circuits is to match the Power Supply with the prime power source. The Prime Power Interface circuits include the distribution and protection circuits that are required to match either a 115 VAC (or optionally 230 VAC), 50 to 60 Hz prime power source to the Power Processor PCB Assembly.

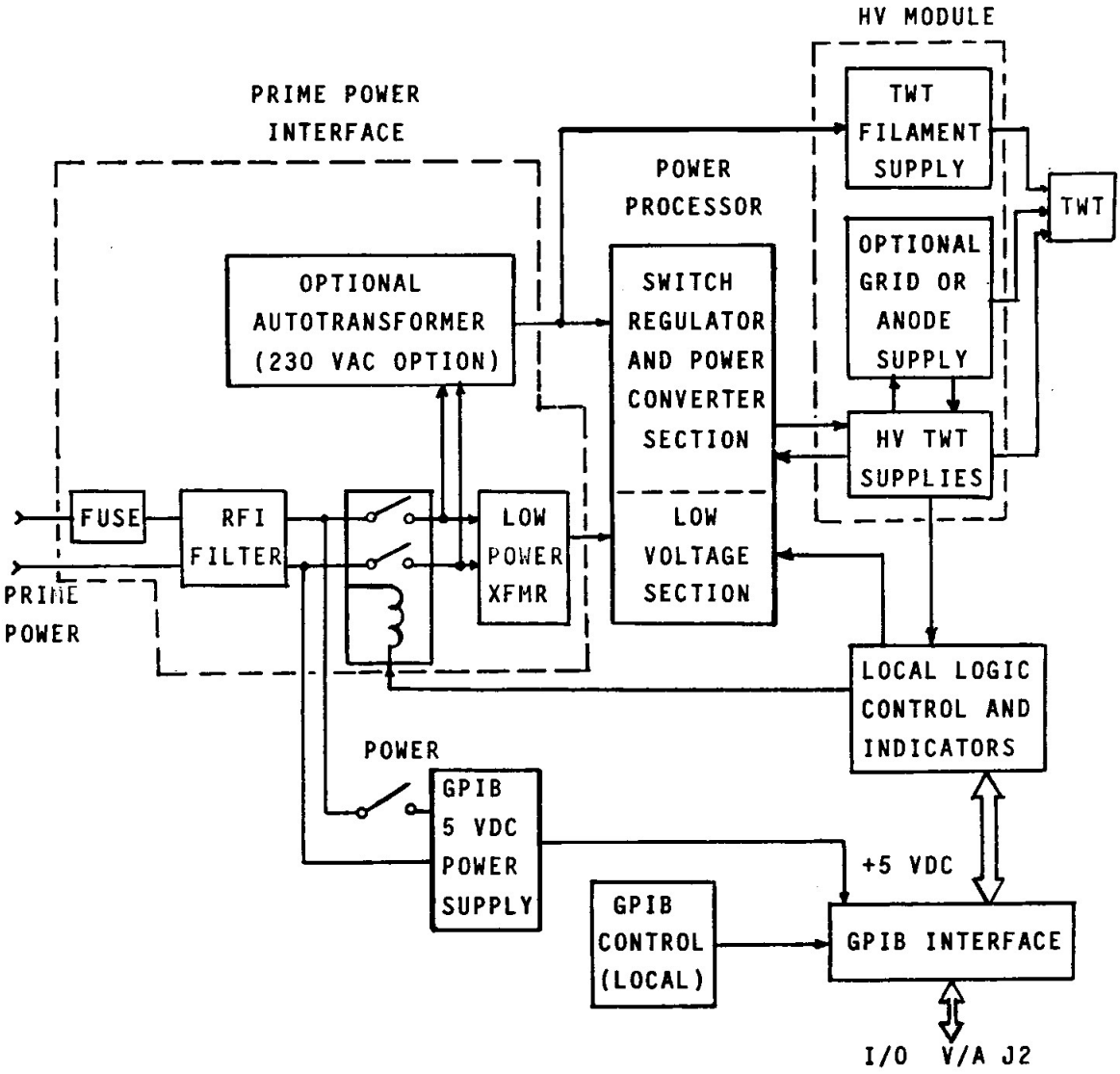


FIGURE 4-2

POWER SUPPLY BLOCK DIAGRAM

4.3.1.1 Standard Configuration. The basic unit is configured to match a 115 VAC, 50 to 60 Hz prime power source to the Power Supply.

4.3.1.2 Optional 230 VAC Operation. When this option is selected, autotransformer T1 and resistor R1 are installed on the Main Chassis Assembly. Refer to schematic Section 6.

4.3.1.3 Fusing. All TWTAs in this series are equipped with an in-line AC fuse and RFI filter. The fuse value is determined by the prime power voltage to be applied. Use a 6.25 Ampere, slow-blow fuse for 115 VAC or a 3 Ampere, slow-blow fuse for 230 VAC operation.

4.3.1.4 Outputs. The outputs of the prime power interface circuits are:

A. 115 VAC for the Switch Regulator, Filament Supply and optional Grid Supply.

B. 18 VAC for the Low Voltage Bias Supplies.

4.3.2 Power Processor PCB Assembly (A2)

NOTE

In the following discussion of the Power Processor Assembly, all reference designations are preceded by 1A2, e.g. the correct designation for R1 on the Power Processor Assembly would be 1A2R1.

4.3.2.1 Function of Power Processor PCB. The Power Processor provides a number of functions as follows:

A. Turn-on surge current limiting by means of a Triac switch and associated control circuit.

B. A bridge rectifier to provide an unregulated 160 VDC bus for the Switch Regulator.

C. A well-regulated 60 to 115 VDC voltage bus needed for the high voltage circuits. A 40 kHz Switch Regulator is used to provide precise voltage regulation and foldback current control. The foldback current limiting circuits restricts short circuit currents to roughly two Amperes and limits Switching Regulator output currents to four to six Amperes, depending on the specific bus voltage selected. The regulation circuits are effective when the Power Processor PCB Assembly is operated alone (i.e. no load condition) or when connected to the High Voltage Assembly.

D. A 20 kHz power converter that chops the regulated bus of the Switch Regulator when the Power Processor is connected to the High Voltage Assembly.

E. A Solid State Feedback Amplifier that senses the high voltage on the tube and adjusts the voltage reference of the Switch Regulator to obtain regulation of the high voltage applied to the tube.

F. An isolated control circuit that allows high voltage to be turned-on or turned-off.

G. A bus monitoring circuit that turns-off high voltage if the Switch Regulator bus exceeds a preset value.

H. A line monitor circuit that monitors the prime power voltage level applied to the TWTA and turns-off the high voltage if the voltage is too low.

I. A capacitor discharge circuit that discharges the capacitor input to the Switch Regulator anytime prime power is turned-off.

J. Regulated low voltage bias supplies needed for the TWTA are as follows:.

1. +15 VDC (referenced to chassis ground) for the cooling fan.
2. +12 VDC (referenced to chassis ground) for the logic and indicator functions and for the HV Feedback Amplifier and turn-on current limiting circuits.
3. ±5 VDC (referenced to the negative rectified line voltage) for the power converter.
4. +12 VDC (referenced to the negative rectified line voltage) for the Switch Regulator and Power Converter.

All of these functions are provided on a single printed circuit board that may be tested as an isolated assembly. Test points for troubleshooting are provided on the board. Two adjustable controls allow this board to be setup for any one of the tubes used in this series of TWTAs.

NOTE

Some of the circuits are not referenced to chassis ground because the power supply is based on the use of an off-line power regulator and converter.

A block diagram of the Power Processor PCB Assembly is shown in Figure 4-3.

4.3.2.2 Turn-On Current Limiting. The function of the turn-on current limiter is to prevent excessive prime power in-rush current during start-up of the TWTA. The Turn-on Current Limiting Circuit is designed to gradually increase the portion of time that AC is applied to full wave rectifier CR9 which is connected across the unregulated bus on the input to the Switching Regulator.

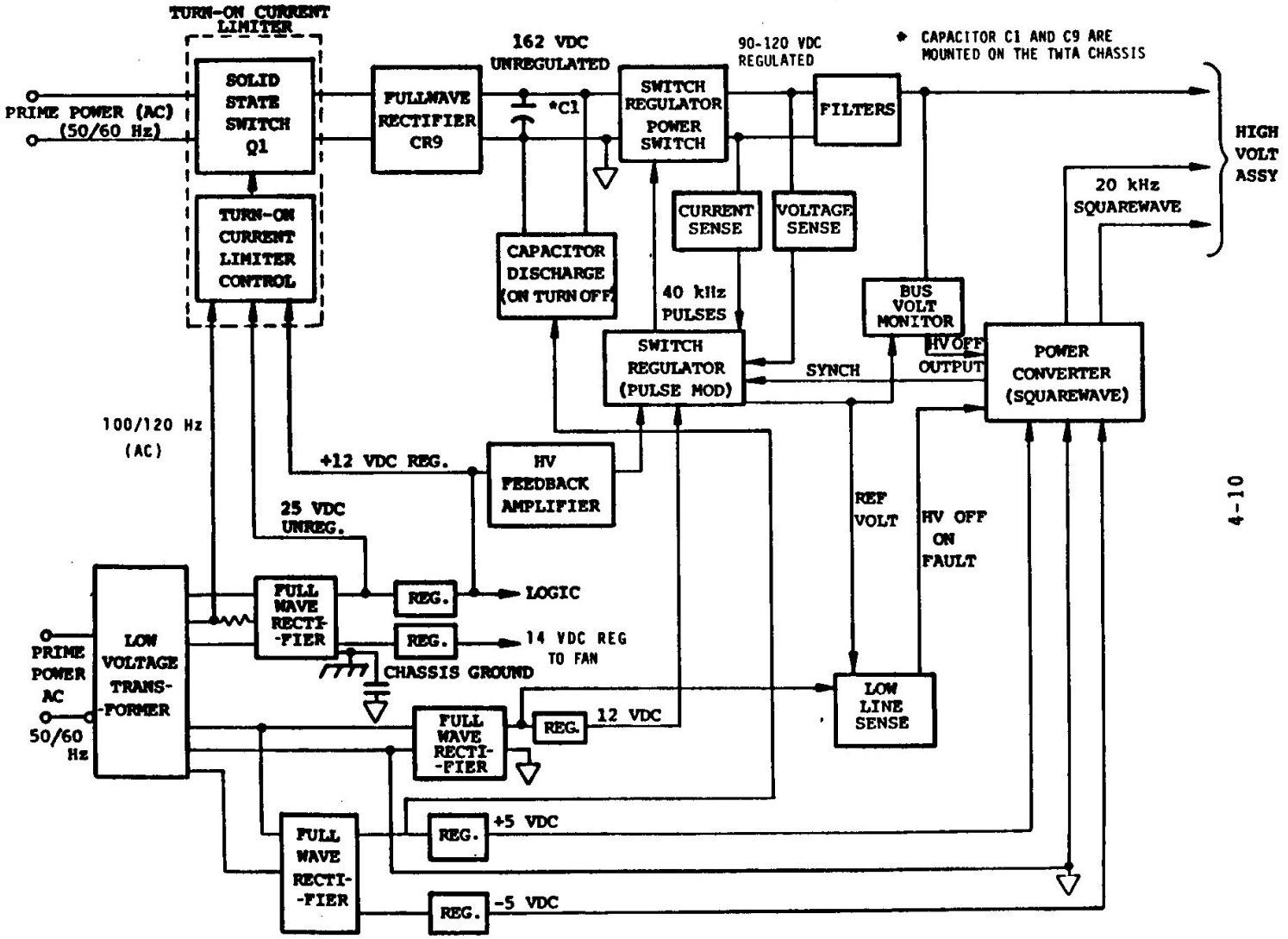


FIGURE 4-3 POWER PROCESSOR PCB BLOCK DIAGRAM

1033-1/85

Figure 4-4 shows the effect of turn-on limiting circuit on the input and output of CR9 during different portions of the start-up cycle. The cross hatched area indicates the time when voltage is actually applied to CR9 and the approximate appearance of the output waveform. A block diagram of the Turn-on Current Limiter is shown in Figure 4-5. The Turn-on Current Limiter consists of:

A. A Power Switch, Triac Q1.

B. A diode bridge (CR10) that allows SCR control (via U8) of an AC signal.

C. An optically-coupled SCR (U8).

D. A control transistor Q2.

E. A phase modulating control circuit (U1A, U1B, U1C, U1D).

Power Switch Q1 is in series with the 115 VAC input to CR9. This switch will conduct when an AC signal of proper polarity is applied to gate G of Q1 (Figure 4-5). Whenever the anode potential of Triac Q1 is removed after it has been gated, Q1 stops conducting. This means that whenever the AC input voltage to Q1 goes to zero, Q1 stops conducting. If the proper AC signal voltage is applied to gate G, Q1 will conduct as long as the magnitude of the in-phase AC input across Q1 is greater than zero volts. The combination of Q2, U8 and CR10 is used to develop the AC gate signal (See Figure 4-6A). For discussion purposes, consider the AC input shown in Figure 4-6 as being divided into half cycle #1 and half cycle #2. As the magnitude of the signal increases during half cycle #1, current I_1 would increase and follow the circuit path shown in Figure 4-6.

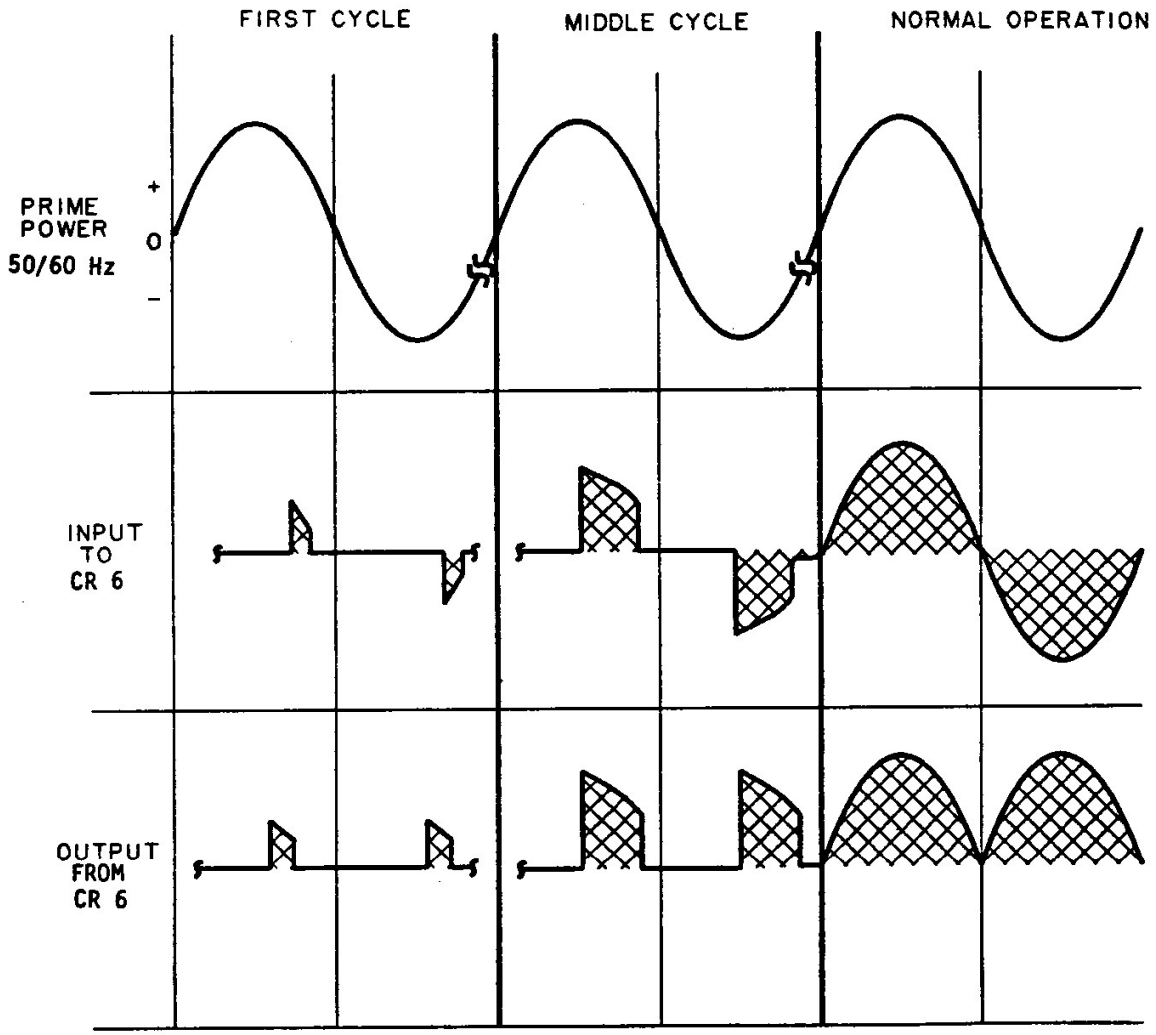


FIGURE 4-4
PULSE WIDTH INCREASE DURING TURN ON

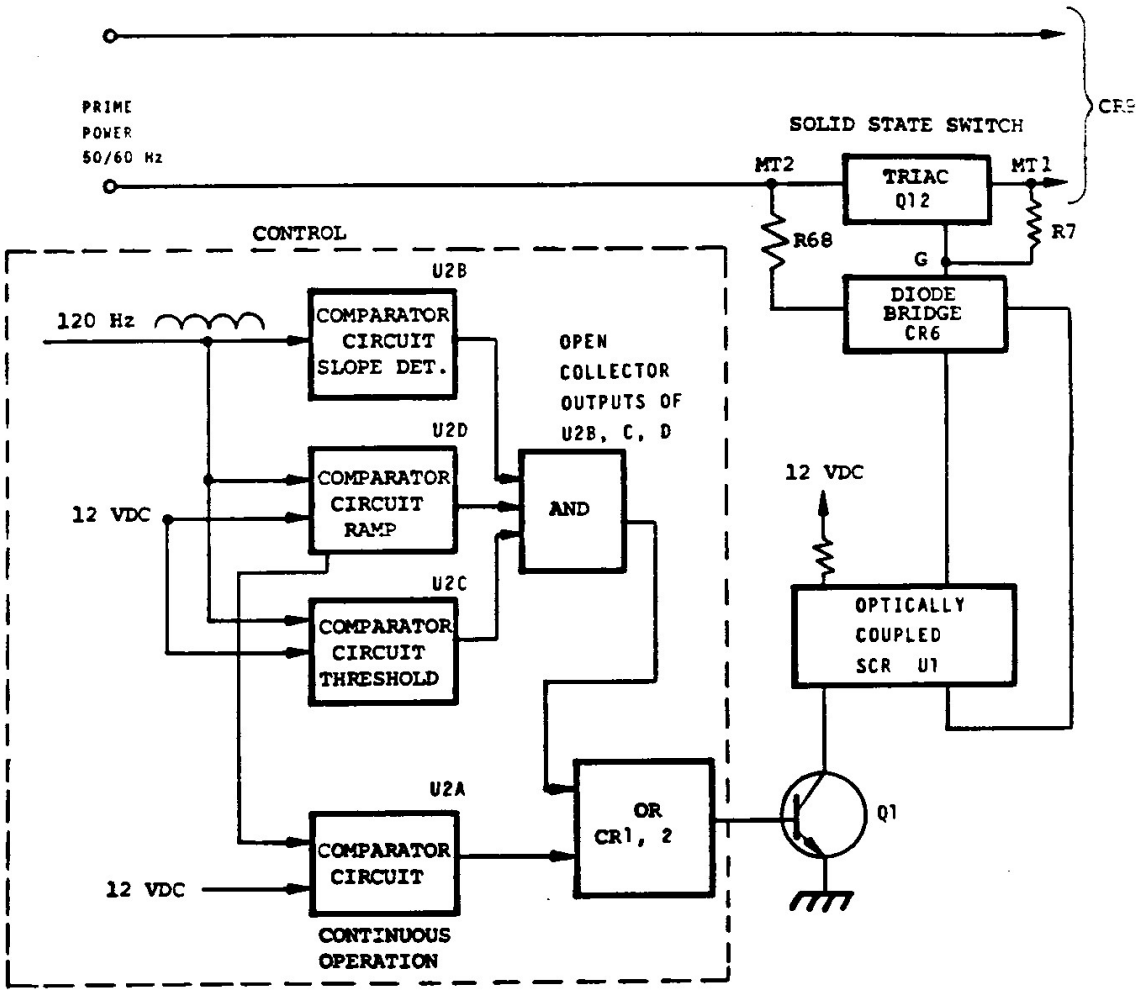
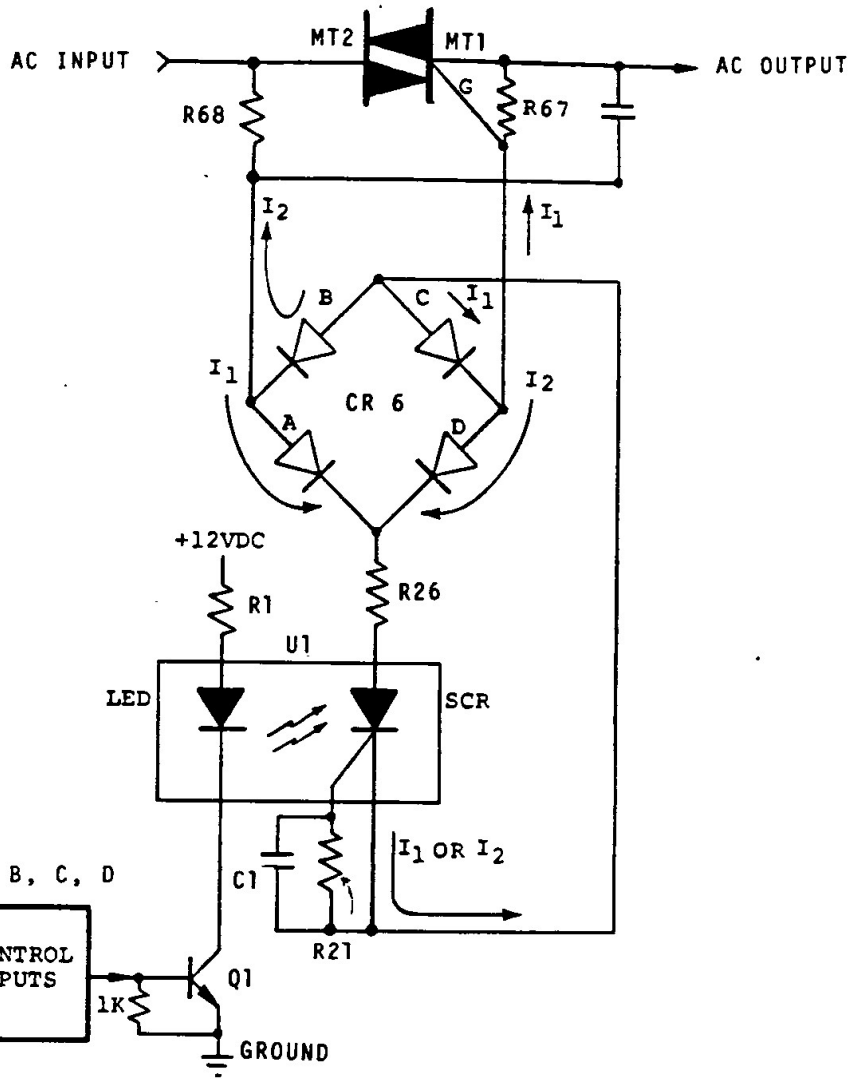
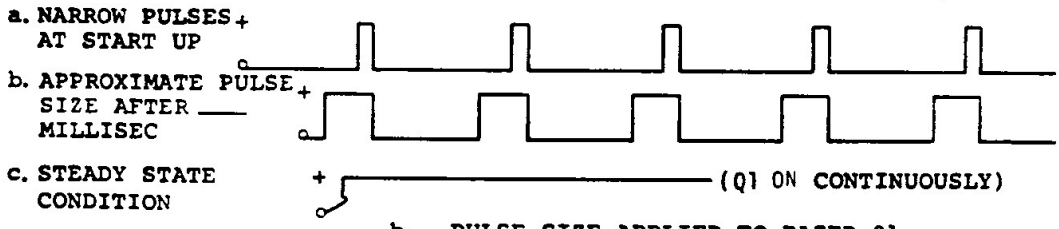


FIGURE 4-5 TURN-ON CIRCUITS

1034-1/85



a. BASIC CIRCUITS FOR GATING TRIAC Q12.



b. PULSE SIZE APPLIED TO BASED Q1.

FIGURE 4-6 POWER SWITCH CIRCUIT OPERATION

1035-1/85

The current path during half cycle #1 would be through R68, diode CR10 A of CR10, R69, the SCR portion of U8, diode C of CR10 and to gate G. During half cycle #2, the current would flow in the opposite direction and through diodes CR10 D and B.

Currents I_1 and I_2 can flow only if the SCR portion of U8 is ON. The SCR portion of U8 acts as a latching switch during each half cycle. The switching action is controlled by the LED portion of U8. Transistor Q2 controls the LED portion of U8. When Q2 is on, current flows through the LED portion of U8 which emits light that actuates the SCR portion of U8 (i.e., U8 is an optically-coupled SCR).

Q2 operation is established by the control input circuits (U1A, U1B, U1C, U1D). The function of the control input circuits is to limit the portion of time that Q1 conducts AC current during each half cycle until the start up cycle is complete and then operate Q2 with a 100% duty cycle. This is achieved by turning-on Q2 with pulses that become longer as a function of time. At some point (steady state operation), a constant DC signal is automatically applied to drive Q2.

The block designated Control Inputs in Figure 4-6 consists of the four different circuits shown in Figure 4-5. These circuits are identified in the Power Processor PCB Assembly schematic as the Slope detector (U1B), the Ramp Detector (U1D), the Threshold Detector (U1C) and the CW Control (U1A). All of these circuits are based on the use of a voltage comparator which has a logic high output when the voltage on the comparator plus (+) input is greater than that on the comparator minus (-) input. Q2 can be turned-on by a logic high from either U1A or the combination of U1B, C and D. The function of U1A (CW Control) is to turn-on Q2 after a preset delay period. When the TWTA is turned-on, the plus (+) input of U1A is pulled to ground by capacitor C3 which is fully discharged at turn-on. The minus (-) input of U1A is tied to the 12 VDC bias through R2. Since the voltage on the minus input is approximately 11.5 V and the voltage on the plus side is zero, the output of U1A is low.

C3 charges at a rate set by R1 and C3 (roughly 100 milliseconds). When C3 is fully charged, CR1 pulls U1A-5 to 12 VDC and the output of U1A goes high which turns-on Q2 on via CR5.

U1B, U1C and U1D form an AND circuit whose function is to gate Q2 on for increasing periods of time until the CW control circuit takes over control of Q2. The outputs of U1B, C and D are open collector circuits that connect to Q2 via CR4.

A. Slope Detector (U1B). This circuit permits a high output during the negative-going portion of each cycle (see Figure 4-7a). Both inputs of U1B are connected to the same 9 VAC, 120 Hz signal. The purpose of R3 and C2 is to introduce a delay on the plus input (U1B-7) to guarantee that U1B will not go high before the beginning of the negative going portion of the AC signal (See Figure 4-7b). C2 holds U1-7 at a value that is lower than U1-6 when the signal is increasing and higher than U1-6 when the signal is decreasing. If U1B operated alone the result would be a pulse like that shown in Figure 4-7B. The signal applied to U1B is taken from the center tap of 1T1 and reflects the action of CR3 which results in a 120 Hz signal as seen by U1B. As a result, the output of U1B would go high on each half cycle of the 50 to 60 Hz input to T1 as shown in Figure 4-7b. Since U1B-1 (an open collector) is tied to the outputs of U1C and D, the waveforms shown in Figure 4-7b are not actually seen during normal operation of the Power Processor PCB Assembly.

B. Ramp Detector U1D. This circuit turns-on U1D for longer and longer periods of time as a function of the charge on capacitor C3. As C3 charges, the voltage on U1D-11 increases. The other input of U1D (U1D-10) senses the same 120 Hz AC line that was sensed by U1B (See Figure 4-7c). This shows the increase in the voltage on U1D-11 in exaggerated terms.

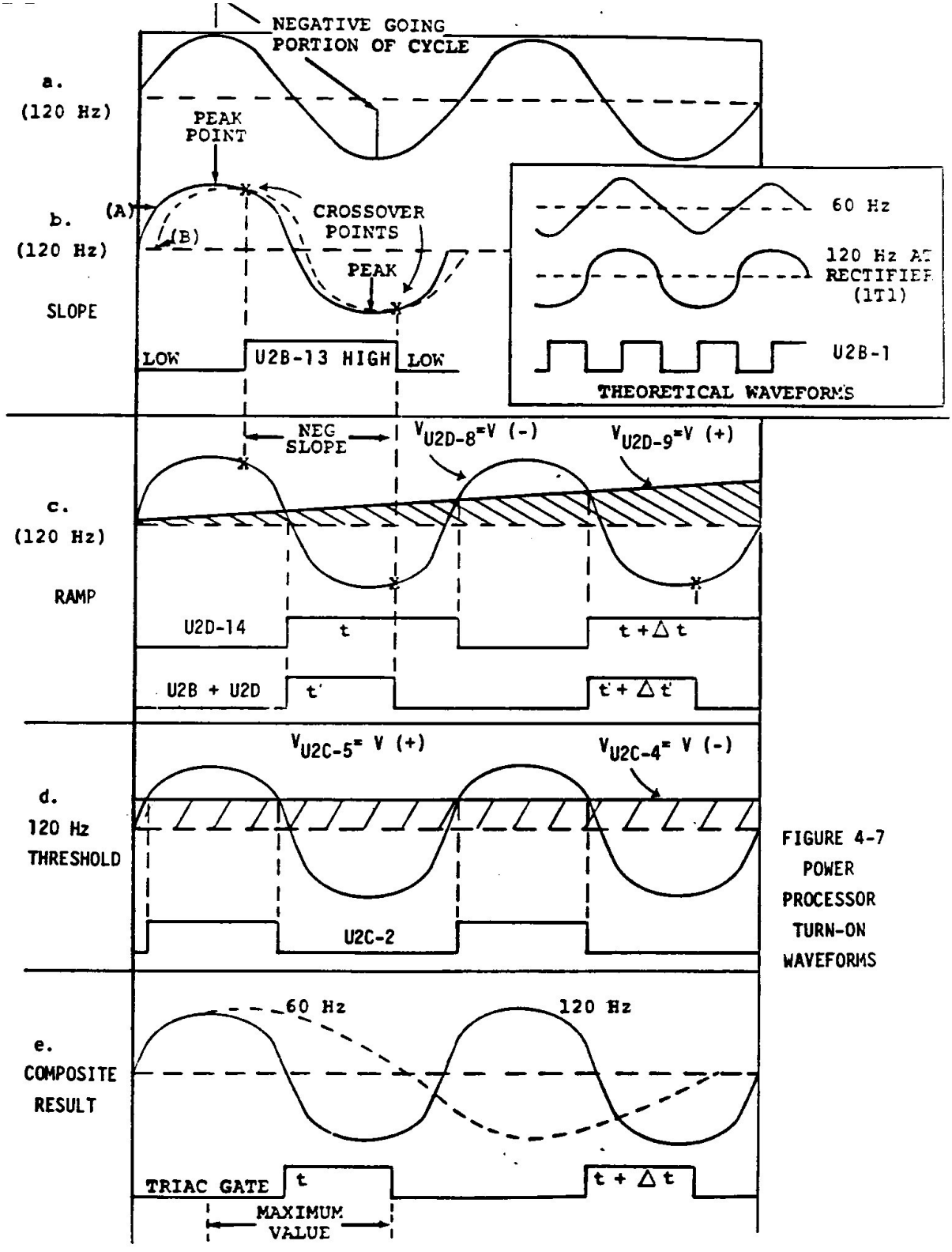


FIGURE 4-7
POWER
PROCESSOR
TURN-ON
WAVEFORMS

Each succeeding cycle V(-) is larger than V(+) for shorter periods of time which results in the output of U1D going high for longer and longer periods of time. Remember that the slope detector only worked a portion of the time (X-Slope-X) in Figure 4-7c. The combined result of U1B and U1D would be a signal similar to Figure 4-7c.

C. Threshold Detector. This circuit limits the time when the output of U1C goes high to a portion of the positive half cycle of each 120 Hz cycle (Figure 4-7d). V(+) senses the 120 Hz signal and V(-) senses the 12 VDC bus. The divider string of R2, R4, R5 is used to reduce the V(-) reference voltage to about 1/2 volt. This keeps the output of U1C low during the zero crossover points of the 50 to 60 Hz prime power cycle.

The composite of the three circuits (U1B, C, D) is shown in Figure 4-7e. The result is a pulse that starts earlier each half cycle of the 60 Hz cycle and cuts off before the zero crossover point of the 60 Hz input. The maximum value of the pulse width is set by the Slope Detector (U1B) to be less than one-fourth of the 60 Hz signal cycle time. The net result is that Q2 is turned-on for very short periods during the early stages of start-up, the periods increase to a value just short of a 50% duty cycle until the CW Control Circuit is actuated and then Q2 operates with a 100% duty cycle. This combination of circuits prevents excessive in-rush current with a minimum of energy losses as compared to dissipative type circuits.

4.3.2.3 Bus Rectifier. A 160 VDC, unregulated, bus is required as an input to the Switch Regulator on the Power Processor PCB Assembly. This bus is generated by the combination of CR9 and capacitor 1C1. (1C1 is mounted on the chassis of the TWTA). The 115 VAC output of the Turn-on Limiter is fed to bridge rectifier CR9 and filtered by capacitor C1.

As a safety measure, C1 is discharged by a special circuit whenever the TWTA is turned off. Figure 4-8 is a simplified schematic of the Bus Rectifier, capacitance filter, and discharge circuit. In normal operation, the combination of R73 and R74 (1K each) bias the base of Q18 to about 6.3 volts and Q18 is turned-on. When Q18 is on, this pulls the base of Q16 low and Q16 and Q17 are off. When the TWTA is turned-off, the unregulated 12.7 VDC bus rapidly decays. When this bus voltage falls below 2 VDC, Q18 shuts off and Q16 and Q17 turn-on. When Q17 is turned-on 1C1 is discharged through R77 (390 ohms).

4.3.2.4 Switch Regulator. The Switch Regulator provides a well regulated, adjustable 60 to 115 VDC bus that is used to drive the High Voltage Assembly. A simplified block diagram of the Switch Regulator is presented in Figure 4-9. The Switch Regulator provides the following:

A. A well-regulated (0.2%) DC bus that is adjustable over the range of 60 to 115 VDC.

B. Regulated Bus output under load or no-load conditions (This is referred to as pre-regulation since overall regulation is obtained by feedback from the high voltage output to the TWT).

C. Current limiting with foldback that limits short circuit currents to two Amperes and normal operating currents to the range of four to six Amperes, depending on the bus voltage selected.

D. Regulation of the high voltages applied to the TWT during normal operation.

Integrated circuit U3 is the focal point of the Switch Regulator. A simplified schematic of U3 is presented in Figure 4-10.

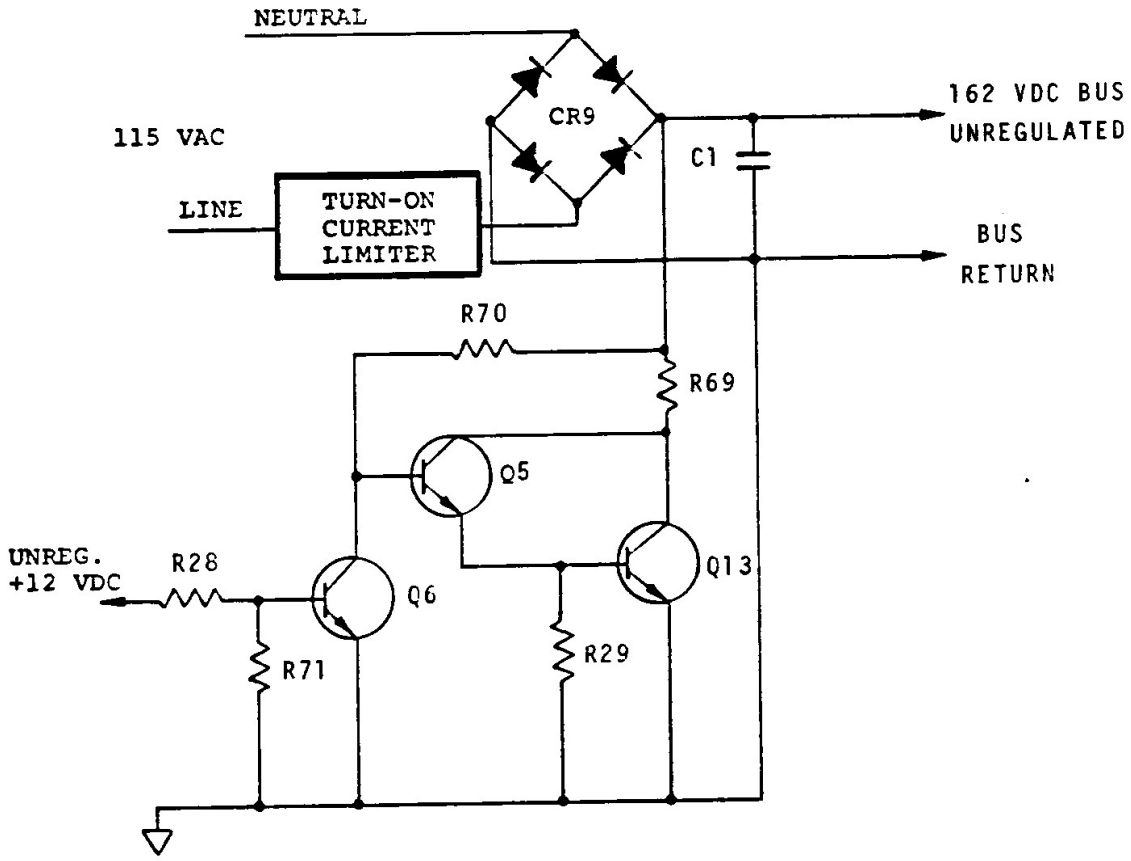


FIGURE 4-8 BUS RECTIFIER SIMPLIFIED SCHEMATIC

1037-1/85

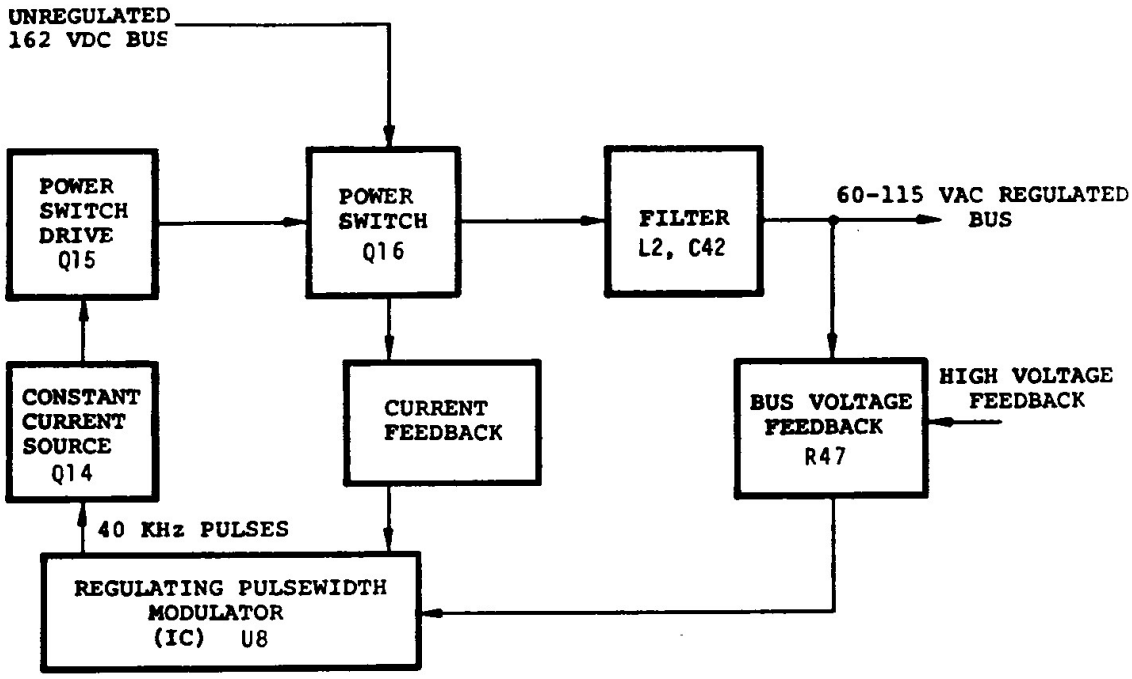


FIGURE 4-9

SIMPLIFIED BLOCK DIAGRAM-SWITCH REGULATOR

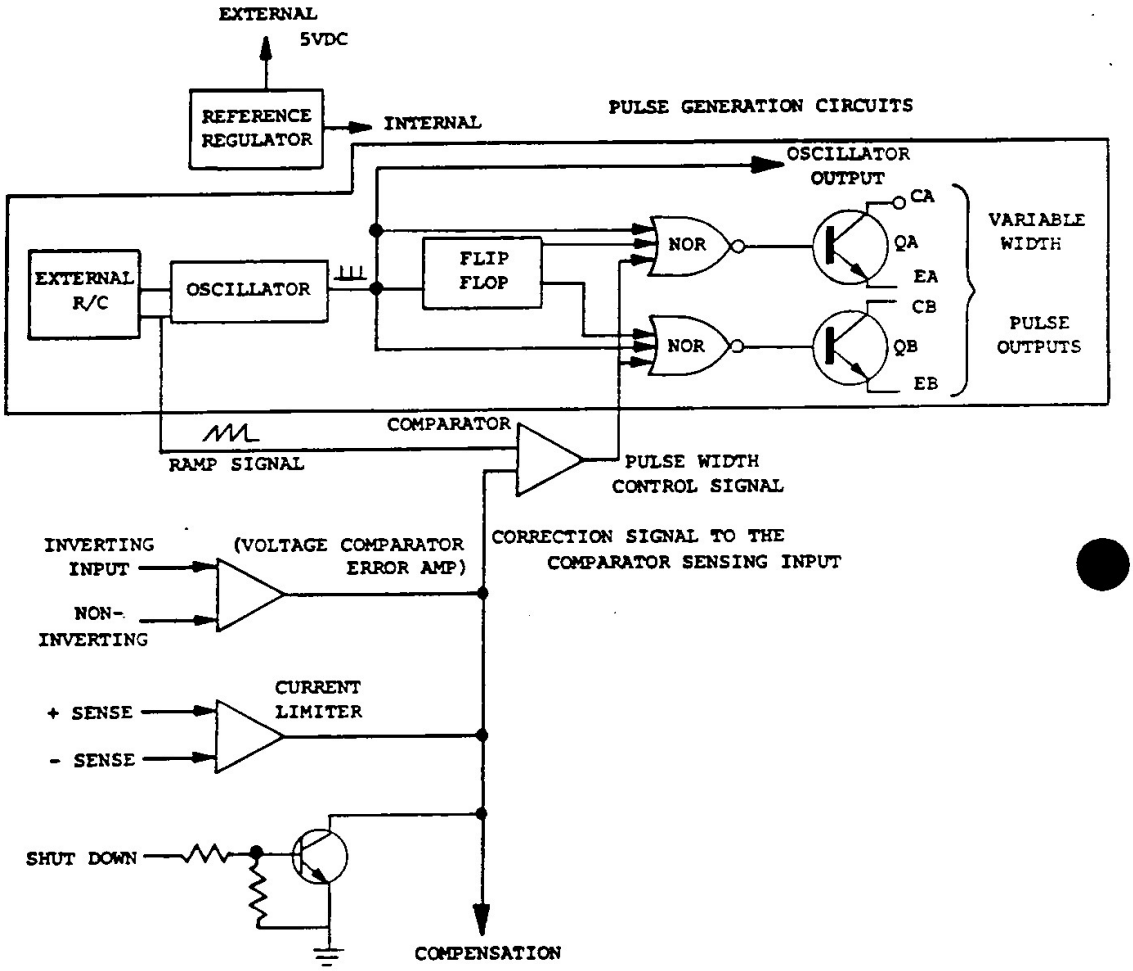


FIGURE 4-10 BLOCK DIAGRAM SWITCH REGULATOR IC

1039-1/85

U3 includes a combination of circuits that produce pulses on the collector/emitter of a pair of transistors that operate 180 degrees out of phase with each other. The frequency of these pulses is established by an internal oscillator which is controlled by an external R/C network. These pulses can be used as separate outputs (e.g. 20 kHz on C_A/E_A and 20 kHz on C_B/E_B) or can be added together to form a pulsed output at twice the frequency (e.g. the two 20 kHz pulse outputs when combined would be 40 kHz.) The width of the pulses is controlled by an internal comparator.

One input of this comparator is driven by the ramp signal that is generated by the internal oscillator. The other comparator input (sense input) is fed to the output of three internal circuits, an error amplifier, a current limiter, and a shut-down circuit. The internal comparator varies the width of the output pulse train in response to signals from the three control circuits.

A low signal on the compensation point (pin 9) from any one of the these three circuits causes the output of the comparator to go proportionally high. This output is inverted by the two NOR circuits feeding QA and QB and turns-off QA and QB until the internal comparator output goes low again. The same IC is used for the Switch Regulator and the Power Converter. In the Switch Regulator, the shut down circuit is not used (SD tied to ground) and the outputs of QA and QB are tied together to provide a 40 kHz pulse train.

U3 is set to oscillate at a frequency lower than that of Power Converter IC U4. The characteristics of this IC are such that if a higher frequency signal is applied to the sync input (pin 3) of U3, the oscillator will be forced to operate at this higher frequency. C19 and R21 set the time constant for U3 and C34 and R55 control U4. Since both capacitors are the same and R21 is 3.9 K while R55 of U4 is 3.32 K, U3 would operate at a rate that is lower than that of U4 if there was no sync signal from U4.

Figure 4-9 shows a 40 kHz output from U3 driving a constant current source (when Q4 is ON) consisting of Q4 and R26. This circuit matches U3 which is a low voltage device with the relatively high voltage unregulated bus and provides immunity to line voltage variations.

Transistor Q3 is used to provide the current amplification needed to operate Power Switch Q5. The combination of L1, R12 and R13, which are associated with Q3, provides for sharp cutoff of Q5 which results in faster switching times and thus higher regulation efficiency.

The primary power switching circuit consists of Q5, and R20. Q3 acts as a switch to turn-on and to turn-off Q5. During the time that Q5 is on, the current delivered to L2 is increasing. When Q5 is turned-off, this current starts to decay. C26 stores the charge delivered via L2. When Q5 is off, the stored energy in L2 starts to release in such a way as to continue the current flow in the same direction in the loop formed by L2, C26, and CR13. Output voltage and output current are sensed to regulate the output bus.

A. Output Voltage Sensing. As mentioned earlier, U3 includes an error amplifier that is used to monitor the bus voltage established by Q5. Figure 4-11 shows a simplified schematic of the Voltage Regulator circuits. The error amplifier reference voltage is set with resistors R35 and R36 to roughly +3.3 VDC, which is applied to the non-inverting input (U3-2) of the error amplifier. The bus voltage is sampled and divided down with resistor string R72 and R33. R33 allows adjustment of the output bus voltage. The sample voltage is applied to the inverting input of the error amplifier via R30. R33 is adjusted to balance the two inputs at the desired output bus voltage.

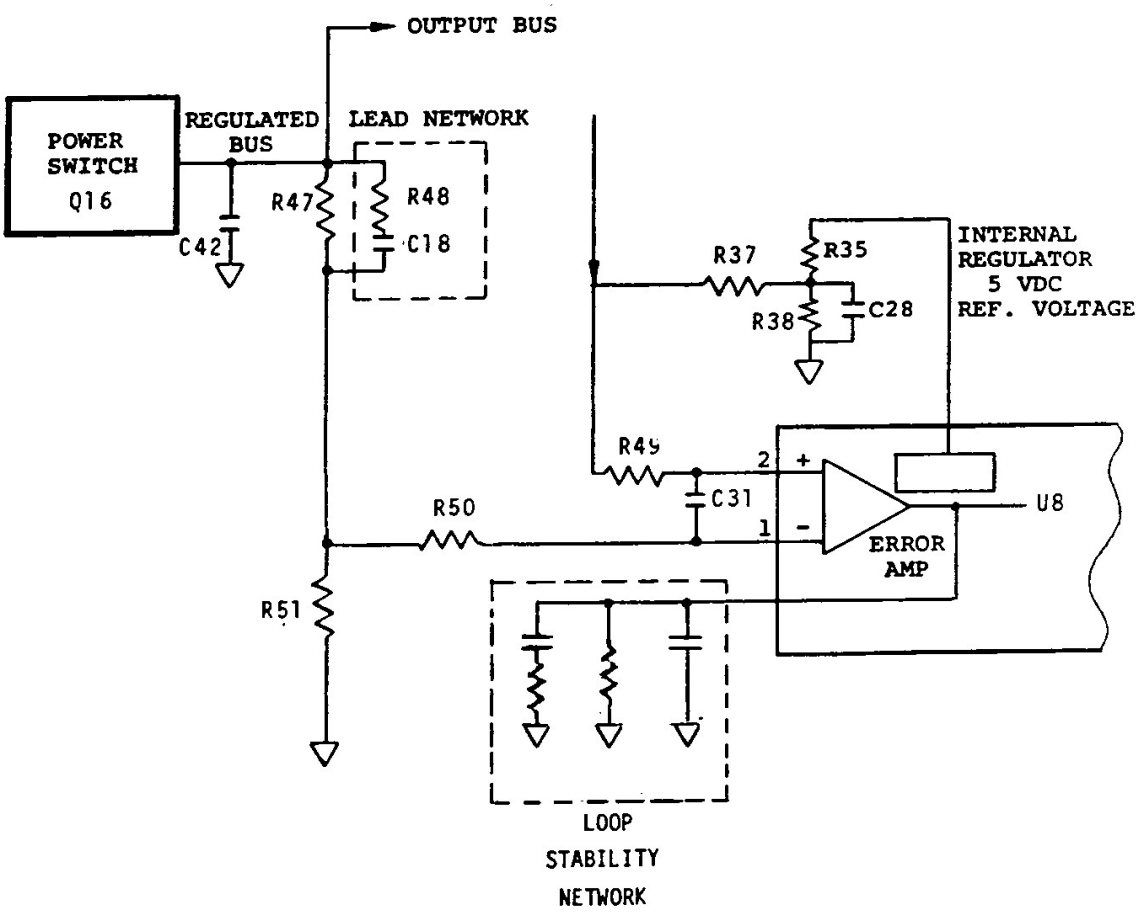


FIGURE 4-11

SIMPLIFIED SCHEMATIC - OUTPUT BUS VOLTAGE REGULATION CIRCUIT

As noted earlier, when the error amplifier output goes high, the pulse width of the drive to the power switch gets longer and when the output goes low the pulse width gets shorter. Therefore, when the sense voltage on R33 goes high, this effect is inverted and the pulse width gets smaller which reduces the bus voltage until the error amplifier inputs balance. Similarly, a decrease in the voltage on R33 results in larger pulse widths until balance is achieved.

The combination of C21, R70, R71, and C42 provide proper loop stability. The combination of R29, C24, and R30 reduce the effects of high frequency noise. R72 and C27 provide a lead network to obtain proper feedback stability.

B. Current Limiting. The Foldback Limiting Circuit limits the current output of the Switch Regulator. This subsequently limits current through the Power Inverter and High Voltage Supplies. In Figure 4-12 the transistor marked QA senses the voltage between point (A) on QA and point (B). ES is selected so that, during normal operation, QA is turned off. When QA is turned on, the width of the pulses from U3 is reduced. QA operates with a built-in threshold of 0.2 VDC.

R25 is used to monitor Switch Regulator current. One ampere equals 0.1 VDC; two amperes equals 0.2 VDC; and five amperes equals 0.5 VDC. If the regulator bus were shorted to the load return, the regulator bus voltage would approach zero and E1 would approach zero. Therefore, the voltage on point A would essentially be that across R25 (E2). As the short circuit current increases above two Amperes, ES becomes approximately -0.2 VDC and QA turns on.

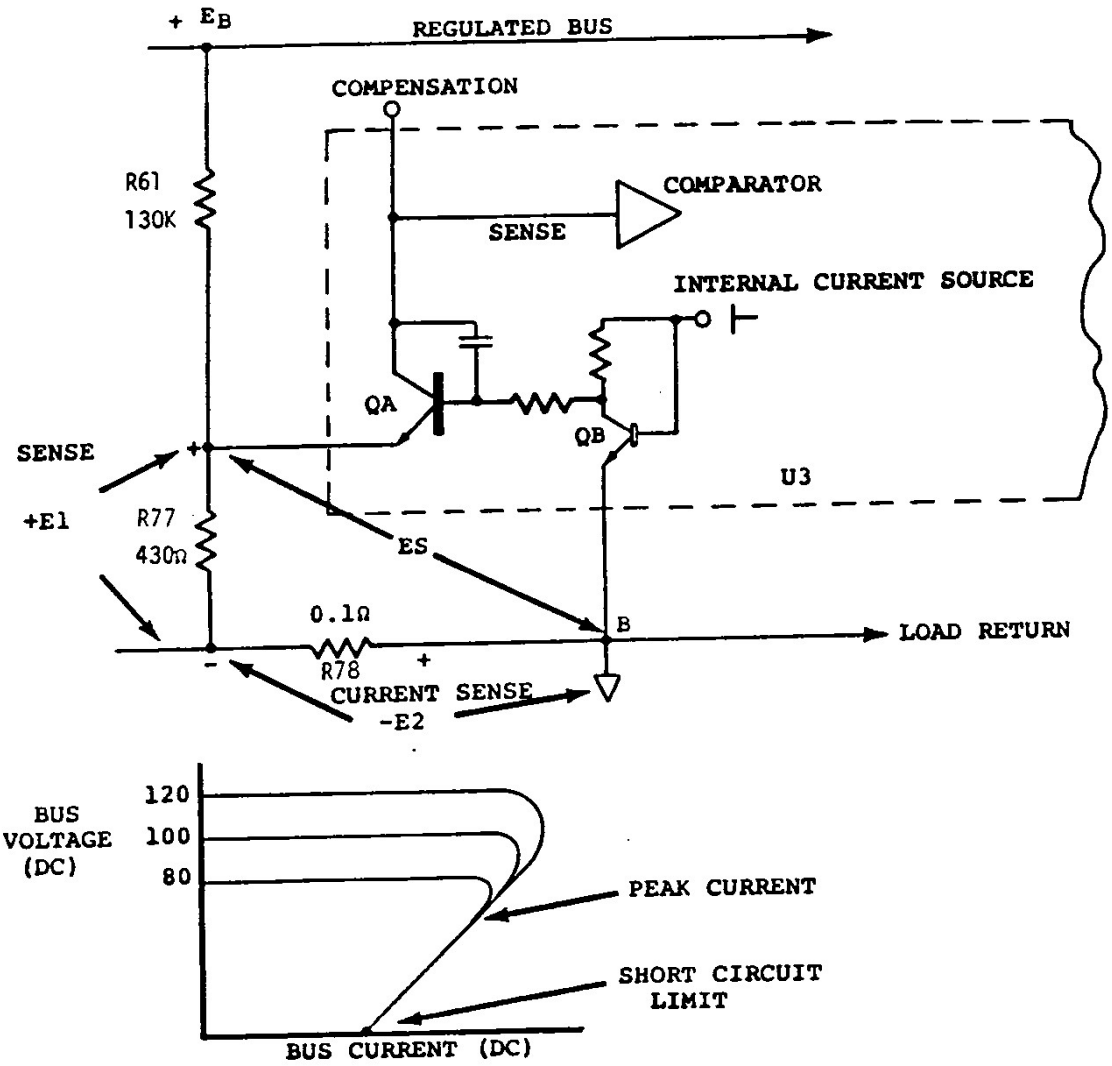


FIGURE 4-12

SIMPLIFIED SCHEMATIC-SWITCH REGULATOR CURRENT LIMITER

This results in a signal to the comparator that in turn reduces the width of the pulse from U3 to the power switch. The result is that Switch Regulator current is limited to about two amperes. When the bus voltage (EB) is not zero, a positive voltage (E1) is developed across R24. Assume that EB is +100 VDC, then voltage E1 would be 0.003 amperes x 100 ohms = +0.3 VDC. Since ES = 0.3 VDC (E1) + (E2) and E2 = -I x R25, the operating current must be at least five amperes if ES is to be -0.2 VDC. When this occurs, U3 pulse widths are reduced which causes a reduction in bus voltage EB. Now it takes less current to keep ES at -0.2 VDC and QA generates a signal to further reduce EB. The result is that the Switch Regulator output current finally drops to two amperes and EBV approaches zero (See the graph in Figure 4-12).
This progressive cycle is known as current foldback, therefore, the current limiter of the Switch Regulator is described as as foldback current limiter. The function of transistor QB (Figure 4-12) is to provide temperature compensation for the current limiter.

4.3.2.5 High Voltage Feedback. This circuit provides direct regulation of the high voltage output to the TWT. The signal from the High Voltage Assembly is compared against an adjustable reference and generates an error signal that can be used to control U3. This circuit also isolates the high voltage feedback signal from the error amplifier of U3.

U9 is the High Voltage Feedback Amplifier. A voltage proportional to the high voltage applied to the TWT is fed back from the High Voltage Assembly to the Power Processor PCB Assembly. The feedback voltage is a few volts above ground potential. This voltage is applied to one input of U9 (pin 2) and compared to the reference voltage on U9-3. The reference voltage on U9-3 can be adjusted over a fairly wide range with resistor R19.

Zener CR11 provides a stable, regulated reference voltage across R19. When the high voltage feedback signal increases or decreases with respect to the balanced condition, the output of U9 will change proportionally. This change is amplified by transistor Q6 and fed to optical coupler U5. The output of U5 is connected to the reference point of the error amplifier of U3. An increase in the reference voltage of U3 drives the bus higher and vice-versa.

4.3.2.6 Power Converter Drive. This circuit converts the regulated DC bus, generated by the switch regulator, into a regulated 20 KHz AC BUS which is then fed to the High Voltage transformer of the High Voltage Assembly. The Power Processor PCB Assembly generates both the regulated DC bus and the low voltage power converter drive signals. The Power Converter transformer is part of the High Voltage Assembly.

U4 is the same type of IC as U3. U4 generates a 20 kHz output on both U3CA and U3CB. This frequency is established by C34 and R55 and is also used to synchronize U3. The combination of R50 and R51 establishes a four-microsecond "dead time" to ensure time separation of the two out-of-phase pulse signals on U3CA and U3CB.

U4 includes a shut-down feature (pin 10). When U4-10 is high, the output of U4 turns off. Op Amp U2 controls the signal on U4-10. ICs U3 and U4 both use an internal +5 VDC reference. The reference voltage of U3 is sensed by U2C (pin 9). The other comparator leg of Op Amp U2C (pin 8) is connected to the output stage of optical coupler U6. When U6 is energized, U6-4/5 acts as a switch and connects U2C-8 to +12 VDC. A high voltage ON command (a logic high) turns-on U6. A logic high on U2C-8 forces the output of U2C low (pin 14) and allows U4 to generate the 20 kHz outputs on U4-CA/Cb. The 20 kHz signals from U4 are fed to two pairs of amplifiers (Q8, Q9, Q10, Q11 and Q12, Q13, Q14 and Q15). The outputs of these stages are two high current 20 kHz outputs that are connected to the High Voltage transformer of the HV Assembly.

4.3.2.7 Line and Bias Voltage Monitors. Low line and bias overvoltage detection circuits are included in the Power Processor PCB Assembly. The sense line of U2D (pin 10) is connected to the output of CR2 (approximately 25 VDC) and dropped to about 6.5 VDC by resistor R39 and R40. The reference input of U2D (pin 11) is connected to the +5 VDC reference of U3. As long as the sense line stays high, the output of U2D (pin 13) stays low and holds Q7 off. If U2D-10 goes low, Q7 turns on, pulls the compensation input (pin 9) of the error amplifier of U4 low, and shuts-off the output of U4. When the output of U2D-2 goes high, it also energizes U7, which generates a low line fault signal that goes to the logic board fault detector.

U2B-6 monitors the switch regulator bus when the bus voltage goes too high (over 115 VDC), the output of U2B-1 goes low which pulls the sense lines of U2A-10 low and the output of U2A-13 goes high which energizes U7.

4.3.2.8 Low Voltage Supplies. The Power Processor PCB Assembly provides the four low voltage bias supplies required for the TWTA. These supplies operate in pairs. Two (+12 VDC and $\pm$5 VDC) are driven by the secondary of transformer T2 and CR2, two (+12, +15 VDC) are connected to output of CR3.

The nominal output of CR2 is 12.7 VDC which is applied to a pair of capacitors (C7, C8) and regulators U11 and U12 to develop +5 VDC and -5 VDC, respectively. The junction of C7 and C8 is tied to the center tap of the secondary of transformer T1 (-7 VAC) which provides the base drive voltages for the converter transistors Q11 and Q12.

The voltage between 1T2-7 and 1T2-8 is applied to a voltage doubler formed by C4, C6 and diodes CR6, CR8, CR7. The output of the doubler is about 25 VDC which is sensed through resistors R39 and R40 by low-line detector U2D-10. This voltage is applied to regulator U10 to develop the 12 VDC bus used to power switch regulator ICs U3 and U4.

The other secondary of 1T2 is connected to CR3 and generates an output voltage of roughly 25 VDC which is fed to regulators U13 and U14. U13 supplies a regulated 15 VDC bus for the cooling fan. U14 provides +12 VDC for the input current limiting circuits, the HV feedback circuits, and the Remote Control interface.

4.3.3 Logic PCB Assembly (A2) Functions

NOTE

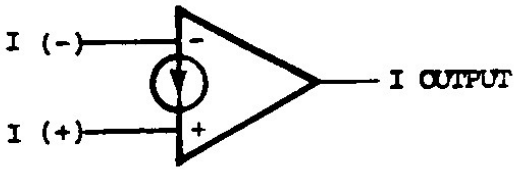
In the following discussion of the Logic PCB Assembly, all reference designations are preceded by 1A3, e.g., the correct designation for R1 is 1A3R1.

The Logic PCB Assembly provides the following functions:

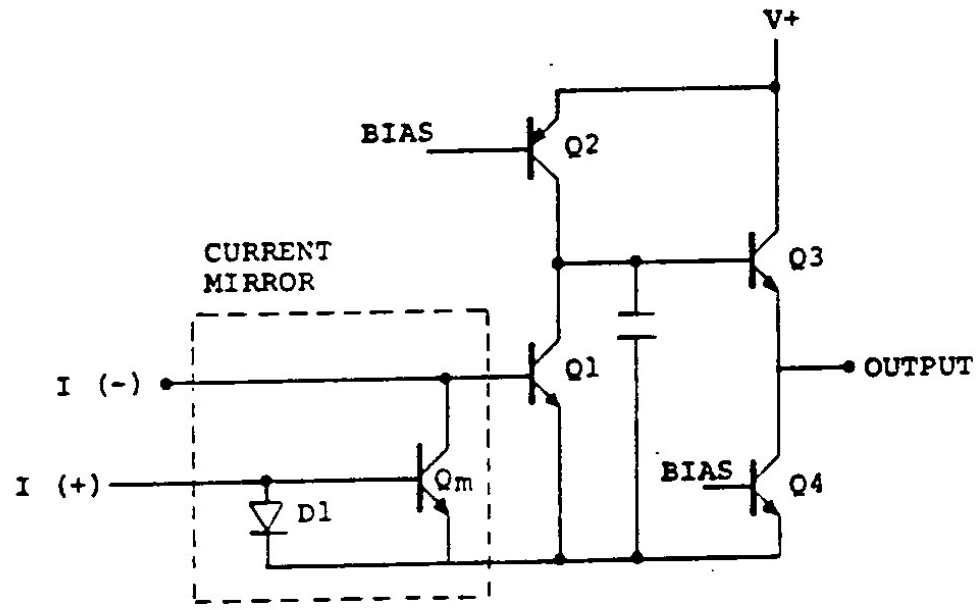
A. Filament Time Delay Timer
B. High Voltage Control
C. Fault Detection
D. Local Status Displays
E. Remote Control and Indicator Interface
F. AC Prime Power Control
G. Local/Remote Operation Mode Selection

Refer to the Fault Logic and Timer schematic (Section 6) for the following discussions.

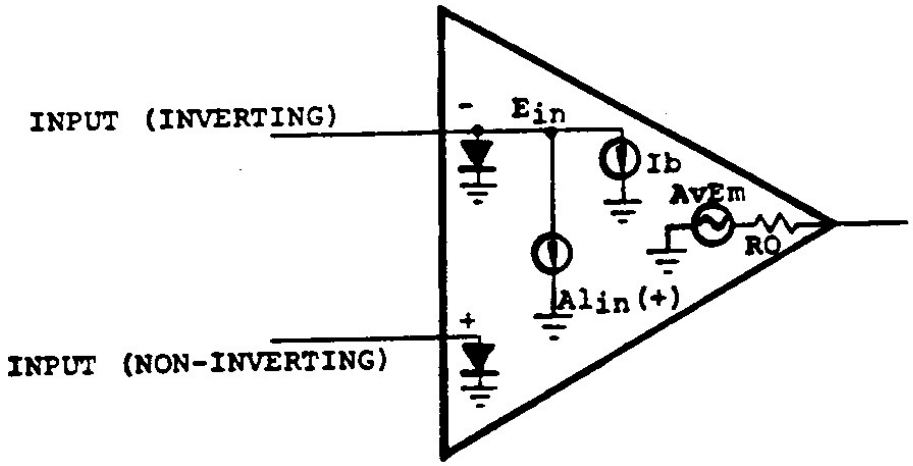
4.3.3.1 Basic Circuit Element. The design of the logic circuits is based on the use of a current differencing amplifier (CDA). The symbol for a CDA is shown in Figure 4-13a. A simplified schematic and equivalent circuit are also shown in Figure 4-13a. The current mirror portion of the circuit (Figure 4-13b) is such that current on the plus side (non-inverting input) acts as a current source at the minus (inverting input). The CDA operates in such a manner that the minus side current equals the plus side current.



a) ENGINEERING DRAWING SYMBOL



b) SIMPLIFIED SCHEMATIC



c) SIMPLIFIED EQUIVELENT CIRCUIT

FIGURE 4-13 CURRENT DIFFERENCING AMPLIFIER (CDA)

1042-1/85

As a result, the voltages at the two inputs of the CDA are essentially constant. This is different from the conventional Op Amp used as comparators where changing voltages are compared. When the CDA input current varies (rather than the input voltages) the CDA output changes state.

In Figure 4-13(c), the minus (-) CDA input is designated as an inverting input while the plus (+) CDA input is designated as the non-inverting input. An increase in current on the plus (+) CDA input (logic high) causes the output of the CDA to go high if the circuit is designed to normally operate with I(+) less than I(-) and will set the CDA output low. In this case, an increase in the magnitude of I(-) does not cause the output to shift. However, if the value of I(-) is decreased to the point where I(-) is less than I(+), the CDA output will go high (i.e. the input on I(-) line is inverted). Consequently, the CDA can be set up for a reference on either leg (depending on whether one wants an inversion of the incoming signal or not).

Resistors in series with the two input lines establish the magnitude of current in each input and to set the threshold for logical output shifts.

The LM 3900, which is the CDA used in the TWTA, consists of four independent, dual input, internally compensated amplifiers which operate with a single power supply and provide a relatively large output voltage swing.

In Figure 4-14, U6A of the Logic schematic is used to monitor the interlock switches. When the normally open cover interlock switch is in the normal operation position, it is held closed by the top cover. This shorts the junction of the 100K resistors controlling the (+) input to the logic supply return. As a result, the input current in the U6A minus leg through the 300K resistor (R7) is greater than that in the plus leg (essentially zero).

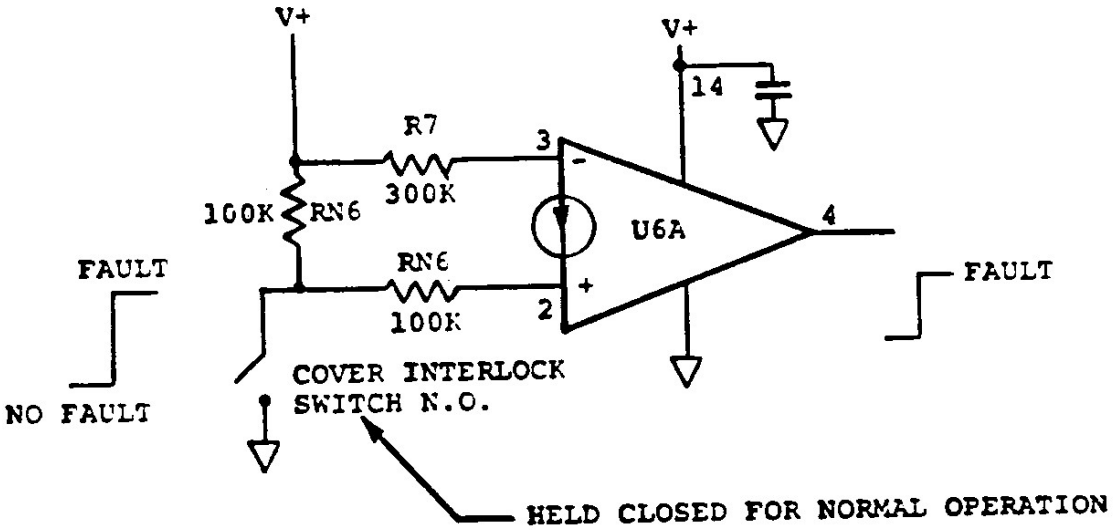


FIGURE 4-14

INTERLOCK CIRCUIT MONITOR LOGIC U6A

If the top cover is removed, the interlock switch opens and allows the (+) leg of U6A to draw more current than the minus leg, I(+) = 1.5 I(-). U6A attempts to drive the current in the minus leg to match that in the plus leg so that the differential current is nearly zero which changes the U6A output from a logical low to a logical high. The U6A output is used to drive the summary fault detector (U1C) and to drive local and remote indicator drive circuits.

4.3.3.2 Filament Time Delay Timer (FTD) The FTD circuits include a Timer (U3A), a clock, and a status detector. The time delay is roughly three minutes which allows the TWT Filament sufficient time to heat up and stabilize. When AC power is applied to T2, 12 VDC is impressed on R11 which controls the current to the (+) input of U3A. At this point I(+) is higher than I(-) and the output of U3A drives positive until the current in IC-7 is equal to I(+). Since C7 is discharged at the time power is applied, I(-) is essentially zero. U3A drives enough current through C7 to keep I(-) equal to I(+). It is, in essence, a constant current source charging C7. The output of U3A (if viewed with respect to time) is a ramp. During the charging cycle, the current in the (+) leg of U3B is less than that in the (-) leg of U3B. The (-) current input to U3B is controlled by variable resistor R14. At a certain point, the current applied to the (+) leg of U3B exceeds that in the minus leg and the output (U3B-5) goes high signifying that the time delay period is over. Adjustment of R14 so that I(-) is lower would result in shorter time delays and vice-versa. When the output of U3B goes high, it drives the current on the sensing input of U1D high which drives the U1D output high and signals the rest of the logic (via CR6 and U1B) that FTD is over.

Whenever the prime power to T2 is on, the current controlled by R11 is a constant value. If prime power is interrupted, I(+) to U3A falls to a value less than I(-) and the output of U3A goes low. When this happens, C7 discharges through U10 at a rate equal to twice the charging rate.

Therefore, if power to T2 is interrupted for 20 seconds and then restored, the FTD circuits will indicate FTD in progress for the 40 seconds it takes to recharge C7. For a three minute cycle, outages of less than 90 seconds will result in proportional delays and as the full three minutes for outages greater than 90 seconds. One should note that prime power to the TWTA is not automatically restored with the AC input voltage. An operator or CPU action via the GPIB is required to command power on.

4.3.3.3 High Voltage Control The HV ON/OFF control signal from the logic to the TWTA supplies is brought out on the output of U4 pin 4. U4 is a multi-transistor chip with transistors used as switches. When these transistors are on, the collector is pulled high (to 12 VDC minus the drop in the transistors), and is used as a control signal or to drive an associated indicator. U4-4 actuates the HV ON/OFF control and indicator U8/16. The signal on U4-6 is controlled by the output of U1B (pin 5). U1B-5 also controls U1A which controls the standby indication. U1A is also connected to the FTD status detector U1D via R13. When the U1B sensing line I(-) signal is inverted, i.e. when the current to U1B-6 goes high, U1B-5 goes low.

NOTE

When the sensing lines go to the I(+) input, a fault is indicated by the line going high and the CDA output going high. When the sensing lines go to the I(-) input, a low on the line indicates a fault and the CDA output goes high.

Each CDA has input resistors to establish the no-fault/fault currents. The resistors (coupling the outputs to the inputs for the non-inverting circuits) provide the proper operating characteristics.

Diodes CR2, CR3, CR4 and CR5 form an OR circuit that is connected to the inverting sense line of Summary Fault Detector U1C (U1C-8). If any one of the fault detectors go high, the output of U1C is driven low.

U1B-6 senses the output of U1D-10 via CR6 and the output of U3D-10 via R10, RN5 (12,3). U3D also has an inverting sense line (U3D-11) that is normally high (HV OFF) and pulled low (HV ON) via the GPIB Interface control line. Only jumper #1 is installed in the K7, K8, and K9 Series TWTAs.

4.3.3.4 Fault Detection Logic. CDA U6C, U6D, U6A, and U3C are used to detect the following individual faults:

FAULT	DETECTOR CDA
Helix Current Overcurrent	U6C
Low Line Voltage	U6D
Interlock Open	U6A
TWT Overtemperature	U3C

4.3.4 High Voltage Assembly (A1)

NOTE

In the following discussion of the High Voltage Assembly, all reference designations are preceded by A1, e.g. the correct designation for R1 is 1A1R1.

The High Voltage Assembly contains the filament (heater) supply and the high voltage supplies.

4.3.4.1 Filament Supply. This circuit provides a regulated bus of 6 to 7 VDC that can operate in conjunction with a high voltage supply. 115 VAC is routed to J5-1, J5-2 from the prime power interface circuits. The AC supply voltage is then distributed within the High Voltage Assembly to J3-12, J3-13 and J4-2, J4-3. Heater transformer T3 is connected to J3-12, J3-13. The secondary of T3 is routed to J3-1, 2, and 3 with J3-1 being connected to the center tap of the secondary of T3. The 18 VAC output of T3 is rectified by CR1, CR2, filtered by C1, C9 and connected to regulator U1. Variable resistor R1 is used to adjust the output to the value (6 to 7 VDC) desired. Diode CR3 provides protection against transients which might be induced by TWT arcs. Capacitor C2 filters the output of U1. Zener VR1 limits the maximum output of U10 to 7.5 VDC.

4.3.4.2 High Voltage Supplies. This set of circuits provide the high voltages for the TWT helix and collector. The helix voltage is determined by the collector and cathode supplies. The output of the Power Processor PCB Assembly is a regulated 60 to 115 VAC, 20 KHz bus which is applied to the primary of high voltage transformer T2.

One secondary of T2 (34, 32, 30) has multiple taps (see schematic 134993) to provide different ratios of HV between cathode to collector and cathode to helix. The selected output is applied to a full-wave, high voltage rectifier consisting of CR8, CR9, CR10 and CR11. The output of this bridge is filtered by C6.

The other secondary (24, 27) provides the cathode to collector voltage. This voltage is applied to a full-wave bridge, consisting of high voltage diodes CR4, 5, 6 and 7. The output of this bridge is filtered by C3. Resistors R4, R5, R6 and R7 are used to limit the secondary currents of transformer T2. The collector voltage is filtered by L1 and C5. A spark gap is connected across Choke L1.

The filtered HV outputs across C3 and C6 are added together to provide the cathode to helix voltage whose magnitude is controlled by 1A2R33 on the Power Processor PCB Assembly.

The cathode voltage is sensed via R19 and fed to the feedback amplifier of the Power Processor PCB. CR12 clamps this feedback point to near ground potential. R19 is in series with two resistors on the Power Processor PCB Assembly, 1A2R18 and 1A2R19. (See Section 3.3.2.5 for a discussion of HV Feedback).

4.3.5 Grid PCB Supply (A5)

NOTE

In the following discussion of the Grid PCB Supply, all reference designations are preceded by A5 e.g., the correct designation for R1 is A5R1.

The Grid Supply is used only with certain tubes and provides regulated positive or negative (with respect to the cathode) voltage, as required. 18 VAC from the High Voltage Assembly is applied (at J1-12, J1-13) to transformer T1. The secondary of T1 is connected to full-wave rectifier bridge CR1 and then filtered by C1. One side of the bridge output is connected to the helix via R11 and R14., The voltage across C1 is impressed on a resistor string consisting of R16, R2 and R1. The voltage across R16 is brought out to the grid and collector through Q2 which controls the magnitude of the voltage. This voltage is selected via variable resistor R7.

4.3.6 Anode Supply (A6)

NOTE

In the following discussion of the Anode Supply, all reference designations are preceded by A6, e.g., the correct designation for R1 is A6R1.

The Anode Supply is a simple, adjustable DC supply. 115 VAC routed via the High Voltage Assembly is fed to transformer T1 via pins J1-2, J1-3. The secondary output is rectified by full-wave bridge CR1 and filtered by C1 to develop a supply voltage of about 480 VDC. The combination of Q1 and Q2 is used to set the current through R1, R2 to establish the desired output voltage. This voltage is adjustable via variable resistor R3 from 0 to 300 VDC. Capacitor C2 provides additional filtering and R6 limits the current that can be drawn by the anode.

4.4 GPIB INTERFACE and CONTROL SECTION

The GPIB Interface Board (01008763) is made up of four main groups of active circuitry: the microprocessor group, the GPIB processor group, the GPIB controller group, and the parallel input/output group.

The microprocessor group consists of the CMOS Z80 CPU, the 6264 RAM, and the 2732 EPROM. The program contained in the EPROM is protected by copyright and may not be reproduced. Since the system clock is 4.9152 MHz, these three chips must be rated for that speed. Technical information for the Z80 is available from the Zilog Corporation.

The GPIB controller group includes the TMS9914A GPIB Controller and the buffers - the 75160 and the 75162. Technical information for these chips is available from Texas Instruments Corporation. The parallel input/output group is made up of ordinary chips. These chips control the filament power and the high voltage. They also light the LEDs and read the status.

The remaining active components on the board are for TTL functions; they provide address decoding and solid state logic. The components are predominately CMOS and are mounted with stand-off sockets. For this reason, little cooling is required and it is possible to put the active components in the space between the ground plane and the "U" formed by the extrusion which makes up the side panel of the amplifier. All of the input and output lines are protected from the electrical noise of the amplifier circuitry by shields, de-coupling capacitors, and pull-up resistors.

4.5 DETAILED DISCUSSION OF RF SECTION

A functional block diagram of the RF Section, including all the standard options, is shown in Figure 4-15. The "6900K7, K8, K9 Series" PAs cover a relatively wide range of frequencies. The specific tube types available are summarized in Table 1-1.

4.5.1 Optional Input Isolator

The optional Input Isolator provides isolation between the input source and the TWT. Typical input VSWR is 1.5 : 1.